DECLARATION FOR TRANSLATION

I, Akio Shiga, a Patent Attorney, of 1-34-12 Kichijoji-Honcho, Musashino-shi, Tokyo, Japan, do solemnly and sincerely declare that I well understand the Japanese and English languages and that the attached English version is a full, true and faithful translation made by me

this 21st day of June, 2004

of the Japanese priority document of

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In testimony thereof, I have herein set my name and seal

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[Title of Invention] EL DISPLAY DEVICE

[Claims]

[Claim 1]

An EL display device in which a plurality of display pixels are arranged, each of the display pixels comprising an EL element having an emissive layer between an anode and a cathode, and a thin film transistor having a source made of a semiconductor film connected to the EL element, wherein

an interface of diffusion region on the source side of the thin film transistor is separated from the emissive layer.

[Claim 2]

An EL display device in which a plurality of display pixels are arranged, each of the display pixels comprising an EL element having an emissive layer between an anode and a cathode, a first thin film transistor having a drain made of a semiconductor film connected to a drain line and a gate connected to a gate line, and a second thin film transistor having a drain made of the semiconductor film connected to a drive line of the EL element, a gate connected to a source of the first thin film transistor, and a source connected to the EL element, wherein

an interface of diffusion region on the source side of the second thin film transistor is separated from the emissive layer.

[Claim 3]

An EL display device in which a plurality of display pixels are arranged, each of the display pixels comprising an EL element having an emissive layer between an anode and a cathode and a thin film transistor having a source made of a semiconductor film connected to the EL element, wherein

a light shielding film for blocking light emitted from the EL element is provided between the EL element and an interface of diffusion region on the source side of the thin film transistor.

[Claim 4]

An EL display device in which a plurality of display pixels are arranged, each of the display pixels comprising an EL element having an emissive layer between an anode and a cathode, a first thin film transistor having a drain made of a semiconductor film connected to a drain line and a gate connected to a gate line, a second transistor having a drain made of the semiconductor film connected to a drive line of the EL element, a gate connected to a source of the first thin film transistor, and a source connected to the EL element, wherein

a light shielding film for blocking light emitted from the EL element is provided between the EL element and an interface of diffusion region on the source side of the second thin film transistor.

[Claim 5]

An EL display device in which a plurality of display pixels are arranged, each of the display pixels comprising an EL element having an emissive layer between an anode and a cathode, a first thin film transistor having a drain made of a semiconductor film connected to a drain line and a gate connected to a gate line, and a second thin film transistor having a drain made of the semiconductor film connected to a drive line of the EL element, a gate connected to a source of the first thin film transistor, and a source connected to the EL element, wherein

a light shielding film for blocking light emitted form the EL element is provided above a semiconductor layer of the first thin film transistor and/or the second thin film transistor.

[Claim 6]

An EL display device according to any one of Claim 3, 4, and 5, wherein

a source electrode or a drain electrode of the thin film transistor also functions as the light shielding film.

[Claim 7]

An EL display device in which a plurality of display pixels are arranged, each of the display pixels comprising an EL element having an emissive layer between an anode and a cathode and a thin film transistor having a source made of a semiconductor film connected to the EL element, wherein

a light shielding film having an opening in a portion corresponding to the EL element is provided below the thin film transistor.

[Claim 8]

An EL display device according to Claim 7, wherein

a light shielding film for blocking light emitted from the EL element is provided above a semiconductor layer of the thin film transistor.

[Claim 9]

An EL display device according to either Claim 7 or Claim 8, wherein

the light shielding film is electrically connected to a drive power supply of the thin film transistor, and

the light shielding film and the source of the thin film transistor are electrically connected.

[Claim 10]

An EL display device according to any one of Claims 7, 8, and 9, wherein

the opening in the light shielding film is formed internal to the emissive layer.

[Claim 11]

An EL display device in which a plurality of display pixels are arranged, each of the display pixels comprising an EL element

having an emissive layer between an anode and a cathode, a first thin film transistor having a drain made of a semiconductor film connected to a drain line and a gate connected to a gate line, and a second thin film transistor having a drain made of the semiconductor film connected to a drive line of the EL element, a gate connected to a source of the first thin film transistor, and a source connected to the EL element, wherein

a light shielding film having an opening in a portion corresponding to the EL element is provided below the thin film transistor.

[Claim 12]

An EL display device according to Claim 11, wherein

a light shielding film for blocking light emitted from the EL element is provided above a semiconductor layer of the first thin film transistor and/or the second thin film transistor.

[Claim 13]

An EL display device according to either Claim 11 or Claim 12, wherein

the light shielding film is electrically connected to a drive power supply of the second thin film transistor, and

the light shielding film and the source of the second thin film transistor are electrically connected.

[Claim 14]

An EL display device according to any one of Claims 11, 12, and 13, wherein

the opening in the light shielding film is formed internal to the emissive layer.

[Detailed Description of Invention]

[0001]

[Field of Invention]

The present invention relates to an electroluminescence display device having an electroluminescence element and a thin film transistor.

[0002]

[Description of Conventional Art]

Recently, electroluminescence (hereinafter simply referred to as "EL") display devices which uses an EL element have attracted much attention as alternative display devices to cathode ray tube (CRT) display devices and liquid crystal display (LCD) devices. For example, many research and development efforts are being dedicated to EL display devices having a thin film transistor (hereinafter simply referred to as "TFT") as a switching element of driving the EL element.

[0003]

Fig. 7 shows a display pixel of an organic EL display device and Fig. 8 shows an equivalent circuit diagram of an organic EL display device. Fig. 9 shows a cross sectional view along the A-A line of Fig. 7 and Fig. 10 shows a cross sectional view along the B-B line of Fig. 7.

[0004]

As shown in these drawings, a display pixel 20 is formed in a region bounded by gate lines GL and drain lines DL. A first TFT 1 which is a switching element is provided near an intersection between a gate line GL and a drain line DL. A source of the TFT 1 also functions as a capacitor electrode 3 which forms a part of a capacitor along with a storage capacitor electrode 2 and is connected to a gate 15 of a second TFT 4 for driving an organic EL element. A source of the second TFT 4 is connected to an anode 6 of an organic EL element and a drain on the other side is connected to a drive line VL for driving the organic EL element.

[0005]

The storage capacitor electrode 2 is formed of chrome or the like, is overlapped with the capacitor electrode 3 which is integral with the source of the first TFT 1 with a gate insulating film 7

therebetween, and stores charges with the gate insulating film 7 as a dielectric layer. This storage capacitor 8 stores a voltage applied to the gate 15 of the second TFT 4.

[0006]

Next, the first TFT 1 for switching will be described referring to Figs. 7 and 9.

[0007]

First, a first gate electrode 11 made of a refractory metal such as chrome (Cr) and molybdenum (Mo) is formed over a transparent insulating substrate 10 made of non-alkali glass or the like. A plurality of these first gate electrodes 11 extend in parallel to each other, for example, to the right and left, integral with the gate line GL as shown in Fig. 7. On the right of the first gate electrode 11 shown in Fig. 9, a storage capacitor electrode 2 formed in the same process as the first gate electrode 11 is formed. In order to form a capacitor 8, the storage capacitor electrode has an enlarged portion between the first TFT 1 and the second TFT 4 as shown in Fig. 7, the enlarged portion being integrally constructed with the storage capacitor line CL extending along the horizontal direction.

[0008]

Then, a first active layer 12 made of a polycrystalline silicon (hereinafter simply referred to as "p-Si") film is formed with the gate insulating film 7 therebetween. The active layer 12 has an LDD (Lightly Doped Drain) structure in which low concentration regions are formed on both sides of the gate, and a source region and a drain region which are doped in a high concentration are formed external to the low concentration regions. A stopper insulating film 13 is formed above the active layer 12. The stopper insulating film 13 is a film for blocking ion doping into the active layer 12 and is formed of an Si oxide film in this structure.

[0009]

An interlayer insulating film 14 in which, for example, an SiO_2 film, an SiN film, and an SiO_2 film are layered in this order

is provided over the gate insulating film 7, active layer 12, and stopper insulating film 13. A drain line DL which becomes a drain electrode is electrically connected through a contact hole C1 provided at a position corresponding to the drain. In addition, a planarizing film PLN made of, for example, an insulating organic resin for planarizing unevenness on a surface is formed over the entire surface. Because an EL display device is current-driven, the EL layer must have a uniform thickness, as the current may be concentrated in a portion with thin thickness. Therefore, because a high degree of flatness is required at least in this formation region of EL layer, the planarizing film PLN is used.

[0010]

Next, the second TFT 4 for driving organic EL element will be described referring to Figs. 7 and 10.

[0011]

A second gate electrode 15 made of the same material as that of the first gate 11 is formed on the insulating substrate 10 and a second active layer 16 is formed with the gate insulating film 7 therebetween. Similar to the above description, a stopper insulating film 17 is provided above the active layer.

[0012]

In the active layer 16, a channel which is intrinsic or substantially intrinsic is formed above the gate electrode 15 and a source region and a drain region with p-type impurity are formed on both sides of the channel to form a p-type channel TFT.

[0013]

An interlayer insulating film 14 described above is formed over the entire surface. A drive line VL is electrically connected through a contact hole C2. In addition, the planarizing film PLN as described above is formed over the entire surface and a source is exposed through a contact hole C3. A transparent electrode (anode of the organic EL element) 6 made of ITO (Indium Tin Oxide) is formed through the contact hole C3.

[0014]

The organic EL element 20 has a layered structure in which the anode 6, a first hole transport layer 21 made of MTDATA (4,4-bis(3-methylphenylphenylamino)biphenyl), a second hole transport layer 22 made of TPD (4,4,4-tris(3-methylphenylphenylamino)triphenylanine), an emissive element layer EM comprising an emissive layer 23 made of Bebq2 (10-benzo[h] quinolinol-beryllium complex) including quinacridone derivative and an electron transport layer 24 made of Bebq2, and a cathode 25 made of an alloy of magnesium and indium are layered in this order. The organic EL element is provided substantially over the entire surface of the organic EL element.

[0015]

The light emission principle and operation of the organic EL element is that holes injected from the anode 6 and electrons injected from the cathode 25 recombine within the emissive layer EM to excite organic molecules forming the emissive layer EM to create excitons. When the excitons radiate and are inactivated, light is emitted from the emissive layer EM and is then emitted to the outside through the transparent anode and the transparent insulating substrate, and the EL element emits light.

[0016]

In this manner, charges supplied from the source S of the first TFT 1 are stored in the storage capacitor 8 and are applied to the gate 15 of the second TFT 4, the organic EL element is current-driven corresponding to the voltage, and light is emitted.

[0017]

[Problem to be Solved by the Invention]

Further developments are expected for the EL element as described above. In order to achieve a high resolution, it is necessary to minimize the size of the pixel and to form as much pixels as possible in a limited region of display pixels.

[0018]

For this purpose, referring to Fig. 7, it is necessary to reduce spacing between various portions such as a spacing between the anode

6 and the second gate electrode 15, a spacing between the anode 6 and the gate line GL of the pixel below, a spacing between the storage capacitor and the anode 6, etc.

[0019]

However, because the EL element is a self-emissive element, there has been a problem in that the emitted light enters the active layer of the TFT, generates a dark current, and causes the brightness to be brighter than the original brightness of the EL element.

[0020]

In addition, in a monochromatic display, for example, there had been a problem in that a portion which should be displayed in gray is displayed with a whiter color.

[0021]

[Means for Solving the Problem]

The present invention was conceived in consideration of the problem described above, and, according to a first aspect of the present invention, the problem is solved by separating an interface of diffusion region on the source side of the thin film transistor from the emissive layer.

[0022]

According to a second aspect of the present invention, the problem is solved by separating an interface of diffusion region on the source side of the second thin film transistor from the emissive layer.

[0023]

When light enters a depletion layer formed near the conjunction interface, the generation of a dark current becomes significant. Although the dark current generated on the side of the drain region is controlled by the gate electrode on the way of the flow to the EL element, the dark current generated on the side of the source region flows to the EL element. Therefore, by also separating, from the EL element, an end of the depletion layer which extends from an interface of impurity within the source region to the side of the anode 6, it is possible to inhibit entrance of light emitted

from the EL element.

[0024]

According to a third aspect of the present invention, the problem is solved by providing a light shielding film for blocking light emitted from the EL element between the EL element and an interface of diffusion region on the source side of the thin film transistor.

[0025]

According to a fourth aspect of the present invention, the problem is solved by providing a light shielding film for blocking light emitted from the EL element between the EL element and an interface of diffusion region on the source side of the second thin film transistor.

[0026]

As described, by forming a light shielding film over the source region of the second TFT which is particularly problematic, it is possible to completely block light.

[0027]

According to a fifth aspect of the present invention, the problem is solved by providing a light shielding film for blocking light emitted from the EL element above the semiconductor layer of the first thin film transistor and/or the second thin film transistor.

[0028]

According to a sixth aspect of the present invention, the problem is solved by the source electrode or the drain electrode of the thin film transistor also functioning as the light shielding film.

[0029]

According to a seventh aspect of the present invention, the problem is solved by providing a light shielding film below the thin film transistor, the light shielding film having an opening in a portion corresponding to the EL element.

[0030]

It is possible to block light entering from the outside through the transparent substrate into the semiconductor layer by the light shielding film and to prevent generation of the dark current.

[0031]

According to an eighth aspect of the present invention, the problem is solved by providing a light shielding film for blocking light emitted from the EL element above the semiconductor layer of the thin film transistor.

[0032]

According to a ninth aspect of the present invention, the problem is solved by the light shielding film being electrically connected to the drive power supply of the thin film transistor and the light shielding film and the source of the thin film transistor being electrically connected.

[0033]

According to a tenth aspect of the present invention, the problem is solved by forming the opening of the light shielding film internal to the emissive layer.

[0034]

According to an eleventh aspect of the present invention, the problem is solved by providing a light shielding film below the thin film transistor and in which a portion corresponding to the EL element is opened.

[0035]

According to a twelfth aspect of the present invention, the problem is solved by providing a light shielding film for blocking light emitted from the EL element above the semiconductor layer of the first thin film transistor and/or the second thin film transistor.

[0036]

According to a thirteenth aspect of the present invention, the problem is solved by the light shielding film being electrically connected to the drive power supply of the second thin film transistor and the light shielding film and the source of the second thin film

transistor being electrically connected.

[0037]

According to a fourteenth aspect of the present invention, the problem is solved by forming the opening of the light shielding film internal to the emissive layer.

[0038]

[Preferred Embodiment]

An EL display device according to the present invention will now be described. Fig. 1 is a plane view of a display pixel in a bottom gate type EL display device. A region surrounded by a dotted line and to which hatching is applied is a region formed of a gate material, a portion surrounded by a solid line and to which no hatching is applied is an Si layer (in the illustrated structure, p-Si layer), a portion surrounded by a solid line and to which a hatching is applied with tilted dots is a portion made of a transparent electrode, and a portion surrounded by solid lines and to which a hatching is applied with tilted lines is a portion formed of an electrode having Al as a primary composition.

[0039]

Figs. 2 and 3 show important points of the present invention and correspond to enlargement views of a portion corresponding to the B-B line of Fig. 1. Fig. 4 is a cross sectional view corresponding to the A-A line of Fig. 1. An equivalent circuit is shown in Fig. 8. A portion surrounded by dotted lines in Fig. 8 indicates a display pixel region.

[0040]

In the present embodiment, a bottom gate type TFT is employed as the first TFT 1 and as the second TFT 4 and an Si film is used as an active layer. In addition, the gate electrodes 11 and 15 each has a double gate structure.

[0041]

The organic EL display device will be more concretely described referring to Figs. 1 - 4.

[0042]

First, there is a transparent substrate 10 which is insulating at least on its surface. In the present embodiment, a metal cap (can) is attached to seal an EL material in order to protect the EL element from moisture. This metal cap, however, is not shown in the figures. Therefore, in order to obtain emission of light from the transparent substrate 10, the substrate 10 must be transparent. If the metal cap can be omitted, it is possible to obtain the emission light from the above, and therefore, the substrate needs not be transparent. In the illustrated structure, a transparent substrate 10 made of glass, synthetic resin, or the like is used.

[0043]

Gate lines GL extends along the horizontal direction above the transparent substrate 10 along an upper edge of a pixel region shown in Fig. 1. In addition, a storage capacitor electrode 2 which functions as a lower electrode of a storage capacitor 8 is formed and storage capacitor lines CL extend along the horizontal direction in order to connect storage capacitor electrodes 2. Because the lines GL and CL are formed in the same layer, these lines are hatched with dots. As the material of these lines, because p-Si is used in the layer above, a refractory metal such as Cr and Ta is used. In the illustrated structure, Cr is formed through sputtering to a thickness of approximately 1000 Å to 2000 Å. The edge is processed to a tapered shape in consideration of the step coverage during the patterning.

[0044]

Then, a gate insulating film 7 and an active layer are layered and formed over the entire surface. In the illustrated structure, the gate electrode and a-Si which is a material of active layers 12 and 16 and a capacitor electrode 3 which is an upper electrode of the storage capacitor 8 are formed through plasma CVD. More specifically, an Si nitride film of approximately 500 Å, an Si oxide film of approximately 1300 Å, and an a-Si of approximately 500 Å are formed through successive plasma CVD in this order from the

bottom.

[0045]

A hydrogen removal annealing is applied to the a-Si within a nitrogen atmosphere of approximately 400 degrees and the a-Si is polycrystallized into p-Si using excimer laser. Reference numeral 13 represents a stopper insulating film made of an Si oxide film which forms a mask when ions are doped into the active layers 12 and 16. When a resist mask is used as the mask, the stopper insulating film 13 is not necessary. The resist mask is removed after doping. Fig. 3 shows a structure when the resist is employed as a mask. Either configuration may be used, but, in general, the two TFTs are used with one of the configurations.

[0046]

P (phosphorous) ions are doped into the first TFT 1 so that N-channel type source and drain are formed and B (boron) ions are doped into the second TFT 4 so that P-channel type source and drain are formed.

[0047]

As shown in Fig. 1, the polycrystallized film is patterned through photolithography. That is, the p-Si layer of the first TFT 1 overlaps the drain line DL near a top left intersection between a gate line GL and a drain line DL, extends above the gate electrode 11, and extends as the capacitor electrode 3 which overlaps the storage capacitor electrode 2. The capacitor electrode 3 extends below the rightmost end of a connection line 30 which is used for electrically connecting to the gate electrode 15 of the second TFT 4. On the other hand, the p-Si layer of the second TFT 4 extends from below the drive line VL at the right side to above the second gate electrode 15, and below the anode 6 made of a transparent electrode.

[0048]

An interlayer insulating film 14 is formed over the entire surface. The interlayer insulating film 14 has a three-layered structure formed through successive CVD of an Si oxide film of

approximately 1000 Å, an Si nitride film of approximately 3000 Å, and an Si oxide film of 1000 Å formed in this order from the bottom. The interlayer insulating film requires at least one layer and the thickness is not limited to those described above.

[0049]

Next, the drain line DL, the drive line VL, and the connection line 30 which are shown hatched with tilted lines in Fig. 1 are formed above the interlayer insulating film 14. A contact is formed, and the semiconductor layer is exposed at a contact hole C1 between the drain line DL and the active layer of the first TFT 1, a contact hole C2 between the drive line VL and the active layer of the second TFT 4, and a contact hole C4 between the connection line 30 and the capacitor electrode 3. Unlike the contact holes described above, because a gate insulating film is additionally layered at a portion corresponding to a contact hole C5 between the connection line 30 and the second gate electrode 15, this layer is further etched to expose Cr. A material of this line has a layered structure of a lower Mo layer of 1000 Å and an upper Al layer of 7000 Å, with the Mo layer functioning as a barrier layer.

[0050]

A planarizing film PLN made of an insulating material is formed to a thickness of approximately 1 μm to 3 μm over the entire surface. One reason for employing the planarizing film PLN is the film for an organic EL as described above in the related art section. This film is made of a first hole transport layer 21, a second hole transport layer 22, an emissive layer 23, and an electron transport layer 24. The hole transport layer may alternatively be formed of one layer. These EL materials are layered structures of very thin films. Moreover, because the EL element is current-driven, these films must be formed with very uniform thickness, otherwise a large amount of current flows through a portion of smaller thickness, which produces a bright point which brightly emits light and, at the same time, causes degradation of the organic film which may lead in the worst case to destruction of the element. Therefore, in order to

prevent the destruction, the overall surface including the anode 6 must be as flat as possible. In the illustrated structure, an acryl-based liquid resin is applied and a flat surface is achieved after curing of the resin. The planarizing film PLN, however, is not limited to this structure.

[0051]

Because the anode 6 and the source of the second TFT 4 are connected in this configuration, an opening is formed in the planarizing film PLN and in the interlayer insulating film 14 and a contact hole C23 is formed through which the second active layer 16 is exposed.

[0052]

An organic film forming a part of the EL element is formed at least above the anode 6. A layered structure is formed above the anode 6, the layered structure including a first hole transport layer 21 made of MTDATA (4,4-bis(3-methylphenylphenylamino)biphenyl), a second hole transport layer 22 made of TPD (4,4,4-tris(3-methylphenylphenylamino)triphenylanine), an emissive element layer EM comprising an emissive layer 23 made of Bebq2 (10-benzo[h] quinolinol-beryllium complex) including a quinacridone derivative and an electron transport layer 24 made of Bebq2, and a cathode 25 made of an alloy of magnesium and silver (Ag), an alloy of Al and Li, or Al/LiF. As the cathode 25, a layered structure of Al and LiF (LiF is formed in very thin thickness and thus, an alloy is substantially formed) is used in the illustrated structure.

[0053]

The anode 6 must be patterned for each pixel. The films above the anode 6 can be formed with the following structures:

I: a first structure in which layers from the anode 6 to the cathode 25 are patterned for each pixel;

II: a second structure similar to I except that the cathode 25 is not patterned and substantially formed common to the entire display

region; and
III: a third structure in which only the anode 6 is patterned for each pixel as shown in Fig. 1 and the layers from the layer immediately above the anode 6 to the cathode are substantially formed common to the entire display region.

The cathode 6, however, typically does not require patterning, and thus is usually formed over the entire surface. In the figures, it is shown that the anode 6 and the cathode 25 are short-circuited, but because the organic film of the EL element is completely covered including the peripheral region of the anode 6, short-circuiting is prevented. This is identical to the related art. Alternatively, it is also possible to form a separate planarizing film in addition to the planarizing film PLN to cover the edges of the anode 6.

[0054]

Then, a metal cap (can) for covering an EL layer of the display region or all EL layers is formed. This is because, when an EL layer absorbs moisture, the EL layer is degraded and therefore, a protection against intrusion of moisture is necessary. Therefore, in order to prevent degradation of the EL layer, a film having a high moisture resistance, for example, a resin film, may be used in place of the cap or a metal cap may be employed in addition to the film having a high moisture resistance.

[0055]

The light emission principle and operation of the organic EL element are that holes injected from the anode 6 and electrons injected from the cathode 25 recombine within the emissive layer EM to excite organic molecules in the emissive layer EM and generate excitons. When the excitons radiate and are inactivated, light is emitted from the emissive layer EM, which is emitted to the outside through the transparent anode and the transparent insulating substrate.

[0056]

A characteristic of the present invention is that entrance of light emitted from the EL element 20, more specifically, from the emissive layer, into the active layer is inhibited.

[0057]

In Fig. 2, hatched regions in the poly Si layer (active layer) 16 are regions to which impurities are doped. Interfaces between the doped regions and I layer are referred to by reference numerals F1, F2, F3, and F4 from the left. In a single gate structure with the two gates integrated, interfaces F2 and F3 will not be present.

[0058]

A first point of the present invention is that the interface F1 of diffusion region is separated from the EL element (in particular, the emissive layer). By separating these structures, it is possible to inhibit entrance of light into the interface of diffusion region. In particular, a depletion layer is created in the interface of diffusion region, and when light enters the depletion layer, generation of dark current becomes more significant. When depletion layer is created at the interface F4 and light enters the depletion layer, for example, a dark current is generated. However, at the drain side, the current flows through the gate electrode to the source region, all current including the dark current are controlled by the gate electrode. The interface F1 on the side of the source region, however, flows directly into the EL element without flowing through the control electrode, and therefore, causes a more serious problem. Thus, it is preferable that the interface F1 be separated as far from the EL element 20 as possible. Figs. 1 and 2 show a structure in which the second gate electrode 15 is shifted toward the drive line VL to separate the interface F1.

[0059]

As structures for preventing light from entering the active layer of the TFT, a light shielding film BM1 shown in Fig. 1 and a light shielding film BM2 shown in Fig. 3 may be employed. The light shielding film BM1 is provided above the first active layer 12 and below the EL element which forms a display pixel at a layer immediately above.

[0060]

The light shielding film BM2 of Fig. 3, on the other hand,

is provided between the EL element 20 and the second active layer 16. In particular, in the illustrated structure, a source electrode SE made of the same material as that of the drive line VL (drain electrode DE) is formed extending towards the right to cover the interface F1. As a result, as shown by the arrows in these figures, the light emitted from the EL element does not enter the interface F1. In addition, as shown with dotted lines, it is desirable that the light shielding film including the interface F4 be formed as close to the drain electrode DE as possible. The light shielding film may alternatively be formed extending from the source electrode SE.

[0061]

The light shielding film BM1 of Fig. 1 is formed in an island-like manner above the active region 12, but may alternatively be formed by extending the drain electrode DE as shown in Fig. 3. Similarly, it is also possible to form the light shielding film BM2 of Fig. 3 in an island-like manner as in Fig. 1.

[0062]

In Fig. 3, at a portion corresponding to the contact hole C3, a contact hole between the source electrode SE and the active layer and a contact hole between the anode 6 and the source electrode are formed.

[0063]

In the above description, the present invention has been described referring to a bottom gate type structure. The present invention, however, can also be applied to a top gate type structure. This configuration will now be described as a second preferred embodiment of the present invention.

[0064]

A planar pattern of the top gate type structure is substantially identical to the bottom gate type structure, and, therefore, Fig. 1 will be referred to. Fig. 5 shows a cross sectional view corresponding to the A-A line of Fig. 1 and Fig. 6 shows a cross sectional view corresponding to the B-B line of Fig. 1. In the

following description, in the figures showing a top gate type structure, two least significant digits of the reference numerals are identical to those in the first preferred embodiment.

[0065]

In a simple description, an insulating layer IL is formed over the entire surface. The insulating layer IL has a layered structure of a lower Si nitride film of 500 Å and an upper Si oxide film of 1000 Å. The Si nitride film functions as a stopper of impurities which elute from glass.

[0066]

Then, an active layer 112 of a first TFT 101, a lower electrode of a storage capacitor 8 formed by extending the active layer 112, and a semiconductor layer (p-Si or a-Si) in a formation region of a second active layer 116 of a second TFT 104 are formed.

[0067]

Then, a gate insulating film 107 is layered over the entire surface, and a gate electrode 111 and a gate line GL integral with the gat electrode 111 are formed above the gate insulating film 107. At the same time, an upper electrode of a storage capacitor 108 is formed in the same layer as the gate electrode with the same material. The upper electrode of the storage capacitor 108 corresponds to the storage capacitor electrode 2 of Fig. 1 and is integrally formed extending along the horizontal direction along with the storage capacitor line CL. As a material of the gate electrode, in addition to the refractory metal materials described above, it is possible to use a material having Al as a primary constituent. A reason that Al may be used is that the interlayer insulating film 114 can be formed at a low temperature through plasma CVD or the like.

[0068]

Impurities are doped into the semiconductor layer which is the active layer with a pattern formed by the gate electrode material as a mask. Because there are a p-channel TFT and an n-channel TFT, one of the TFTs is masked by a resist (this is also done in the

configuration in the bottom gate type structure). After the semiconductor layer is doped with impurities, the semiconductor layer is patterned. The semiconductor layer below the storage capacitor electrode 102 is not doped with impurities. However, a voltage applied to the first gate electrode 111 or a voltage greater than this voltage is applied to this portion to generate a channel in the semiconductor layer, so that this portion is used as an electrode.

[0069]

After the interlayer insulating film 114 is formed, a drain line DL and a drive line VL are formed. Then, planarizing film PLN is formed above the drain line DL and the drive line VL and a transparent electrode is formed as the anode 106 after the planarizing film PLN is formed. A contact C3 between the anode 106 and the second TFT 104 is similar to that shown in Fig. 3 and a source electrode SE is formed in the same layer as the drive line VL. The light shielding film BM2 may be formed such that the source electrode SE covers the active layer, may be formed in an island-like manner as shown in Fig. 6, or may be formed extending from a drain electrode. It is also possible to not employ the light shielding film BM2 and to separate as in Fig. 2.

[0070]

The light shielding film BM1 in Fig. 5, on the other hand, may be formed extending from the drain line DL (drain electrode) or in an island-like manner as shown in Fig. 6.

[0071]

The EL element 20 is identical to that in the first preferred embodiment and will not be described again.

[0072]

In either the top gate type structure or the bottom gate type structure, it is possible to provide a light shielding film to prevent entrance of external light from below the transparent substrate.

[0073]

Although not shown in figures, this light shielding film is

directly adhered on the transparent substrate 10 (110) and has an opening formed therein to allow the EL element 20 (anode 6) to be exposed. As a material of the light shielding film, it is desirable to use a refractory metal material, and, in the preferred embodiments, a Cr layer having a thickness of 1000 Å - 2000 Å is used. In consideration of insulation from the upper conductive material or active layer, an insulating layer is formed. For example, an Si nitride film of 500 Å and an Si oxide film of 1000 Å are layered from the bottom.

[0074]

The light shielding film BM has an opening for exposure in a portion corresponding to the anode 6 (106) and is formed over substantially the entire surface except for the opening. Because of this, entrance of external light can be prevented in portions other than the opening and, thus, dark current can be prevented also in this manner.

[0075]

In addition, the resistance value of the light shielding film is very small and a variation in the resistance is also very small. Therefore, by electrically connecting the light shielding film to the drive line or by electrically connecting the light shielding film to a power supply input terminal T, the voltage applied to each pixel becomes more uniform compared to the conventional structures. The drive power supply input terminal T is connected to a drive power supply.

[0076]

As is clear from the equivalent circuit shown in Fig. 8, the drive line VL extends along the column direction within the display region, is connected to each of display pixels in the column direction, and supplies a drive current. The display region has a significant length and, thus, has some resistance, but because the display region is connected to the light shielding film BM, a voltage at a substantially same potential is applied to adjacent display pixels. In addition, current will also be supplied from the light shielding

film BM so that current which should be supplied to the organic EL element provided in each display pixel can be supplied. Thus, display degradation by the resistance in the display region as described above and reduction in brightness of display can be prevented.

[0077]

Next, the number of contact holes in the light shielding film will be described. A reduction in resistance can be inhibited by forming at least one contact hole over the entire region of the light shielding film. However, by forming a constant and same small number of contact holes in each pixel, it is possible to achieve more uniform distribution of resistance and more uniform distribution of voltage, which allows for more faithful reproduction of the current to be supplied, that is, brightness of light emission.

[0078]

In the above-described preferred embodiments, a p-Si film is used as the semiconductor film. However, it is also possible to use a microcrystalline silicon film, an amorphous silicon film, or the like in the semiconductor film.

[0079]

In addition, because the light shielding film BM is formed internal to the anode, the non-emissive region is not created internal to the opening OP. Therefore, it is possible to clarify a region around a pixel in which light is emitted, and, at the same time, to reduce the area of the opening so that the resistance of the overall light shielding film BM can be further reduced.

[0080]

Although the above-described embodiment is described referring to an organic EL display device, the present invention is not limited to an organic EL display device and may be applied to, for example, an inorganic EL display device in which the emissive layer EM is made of one or more inorganic materials, to achieve similar advantages.

[0081]

In the above description, two TFTs are provided in each pixel. Alternatively, it is also possible to drive each EL element with one TFT.

[0082]

[Advantages]

As is clear from the above description, by separating an interface of diffusion region on the source side of a thin film transistor from an emissive layer (or anode), it is possible to inhibit entrance of light emitted from the EL element into the interface (or depletion layer).

[0083]

By providing a light shielding film for blocking light emitted from the EL element in a region between the EL element and the interface of diffusion region on the source side of the thin film transistor, it is possible to inhibit entrance of light emitted from the EL element into the interface (or the depletion layer).

[0084]

By configuring such that a source electrode or a drain electrode of the thin film transistor also functions as the light shielding film, it is possible to form the light shielding film without adding a separate process.

[0085]

By providing a light shielding film positioned below the thin film transistor and having an opening in a portion corresponding to the EL element, it is possible to block light entering from below the transparent substrate and to inhibit generation of dark current due to the entering light.

By providing a contact hole in each display pixel, it is possible to inhibit unevenness among substantially all display pixels.

[0086]

By connecting the light shielding film and the drive power supply and electrically connecting the light shielding film and the drain of the second TFT, it is possible to inhibit a variation in the resistance due to generation of a resistance component along

the extension direction of the drive line which occurred in the conventional art. It is also possible to omit the drive line.

[0087]

Therefore, although conventionally the color reproducibility of intermediate colors is lost such as in a case in which a portion which should have been displayed in gray is displayed in a whiter color, with the present invention, the dark current is inhibited and the color reproducibility of the intermediate colors is improved. Because a light shielding film having an opening corresponding to a portion of the EL element (emissive layer) is employed, each pixel is clearly displayed, and, thus, the clearness of the image can be improved and mixture of colors can be prevented.

[Brief Description of Drawings]

[Fig. 1]

A plan view of a display pixel in an EL display device according to the present invention.

[Fig. 2]

A diagram showing a second TFT shown in Fig. 1.

[Fig. 3]

A diagram showing a second TFT shown in Fig. 1.

[Fig. 4]

A cross sectional diagram along an A-A line in Fig. 1.

[Fig. 5]

A cross sectional diagram corresponding to a cross section along the A-A line of Fig. 1 and showing an EL display device which uses a top gate type TFT.

[Fig. 6]

A cross sectional diagram corresponding to a cross section along the B-B line of Fig. 1 and showing an EL display device which uses a top gate type TFT.

[Fig. 7]

A plan view of a display pixel of a conventional EL display device.

[Fig. 8]

An equivalent circuit diagram of a conventional EL display device.

[Fig. 9]

A cross sectional view along an A-A line in Fig. 7.

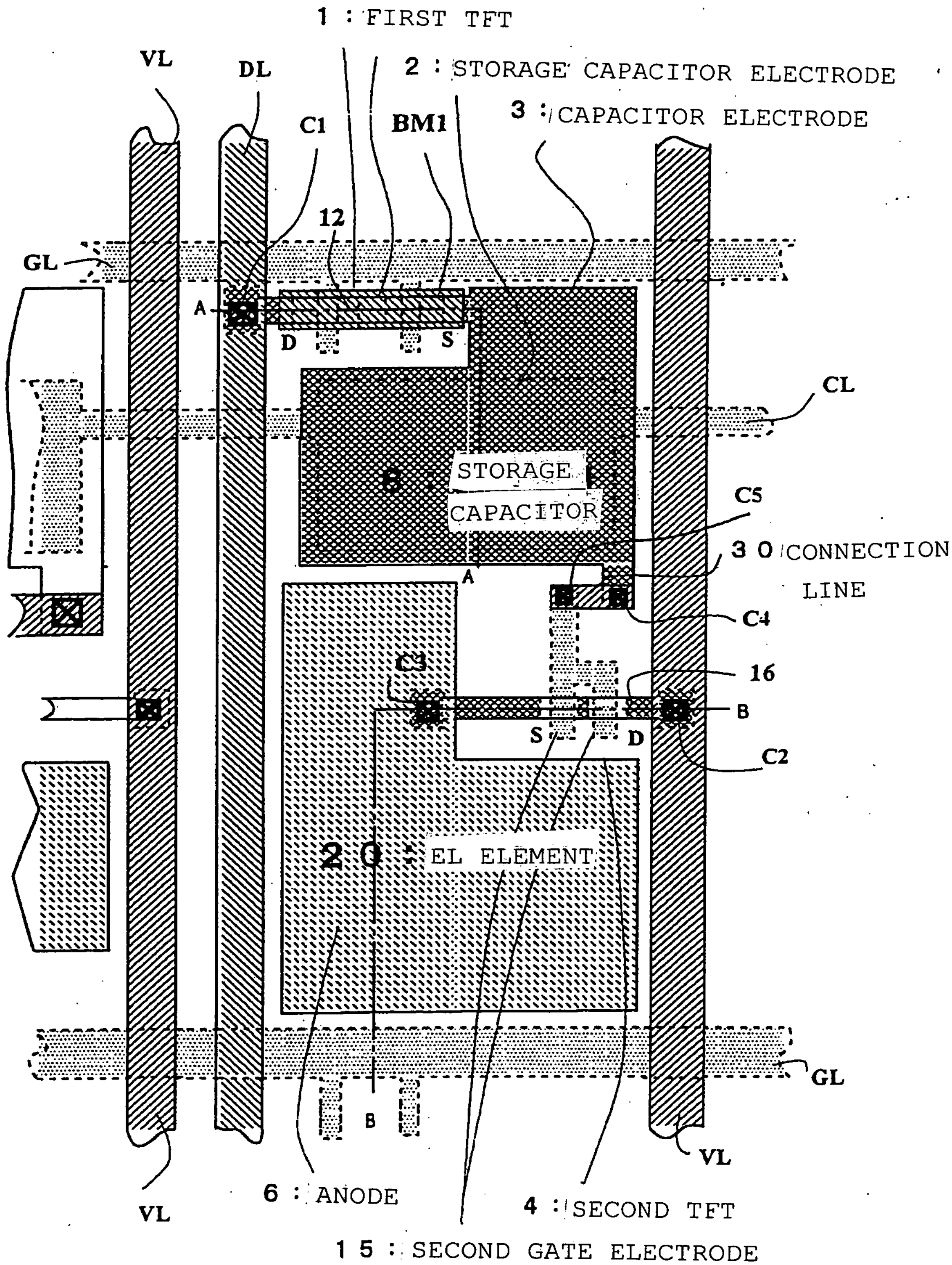
[Fig. 10]

A cross sectional view along a B-B line in Fig. 7.

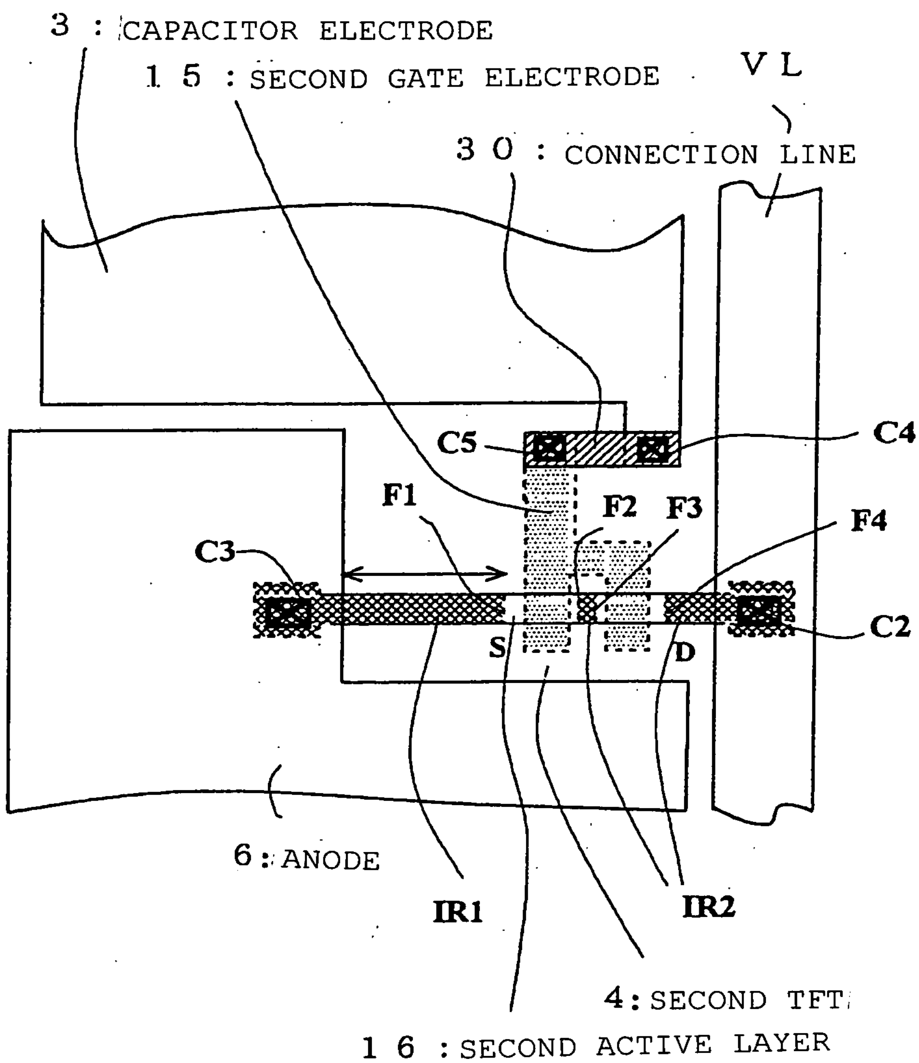
[Explanation of Reference Numerals]

1	FIRST TFT
2	STORAGE CAPACITOR ELECTRODE
3	CAPACITOR ELECTRODE
4	SECOND TFT
6	ANODE
7	GATE INSULATING FILM
8	STORAGE CAPACITOR
14	INTERLAYER INSULATING FILM
20	EL ELEMENT
GL	GATE LINE
DL	DRAIN LINE
CL	STORAGE CAPACITOR LINE
VL	DRIVE LINE VL
BM	LIGHT SHIELDING FILM

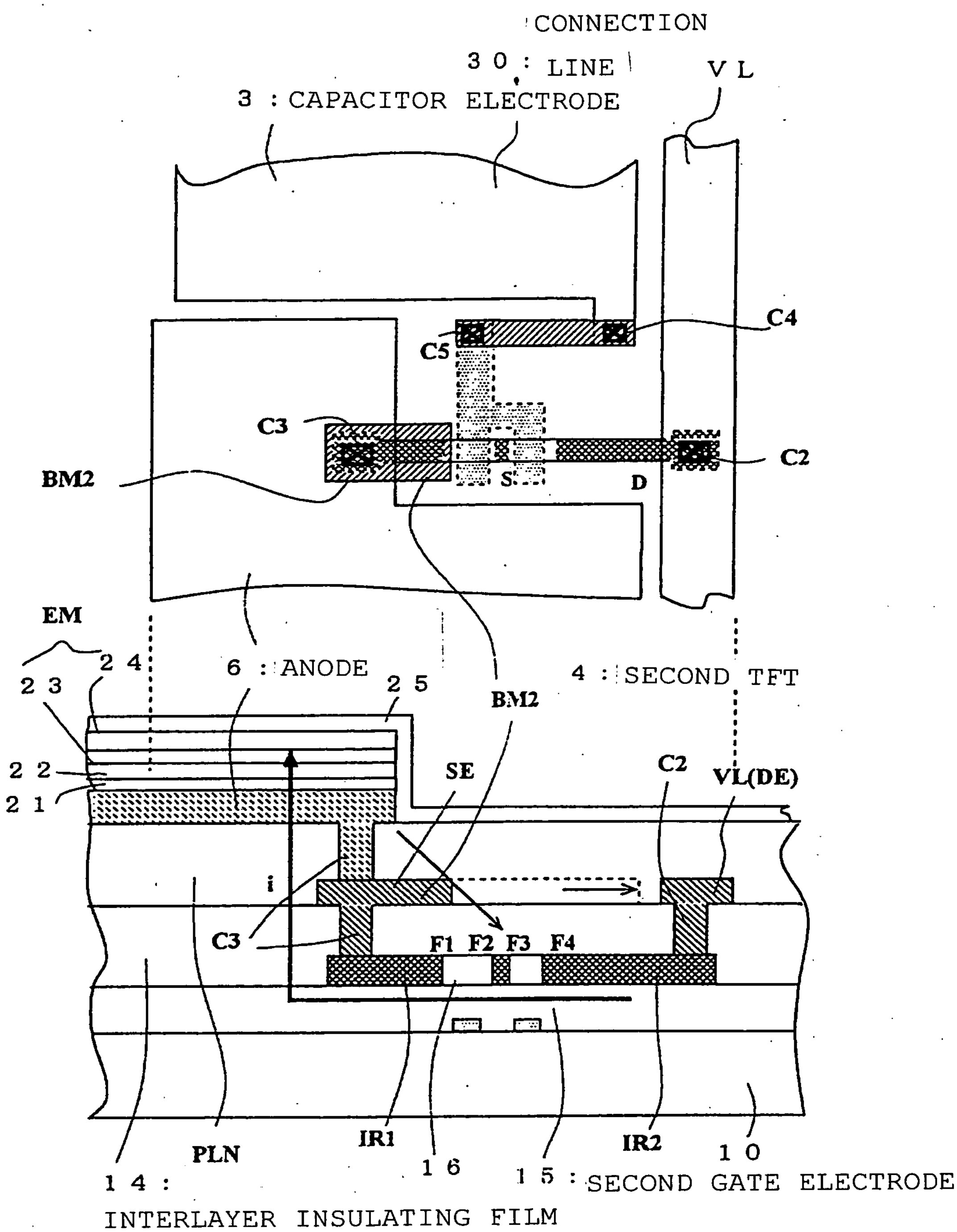
[Fig. 1]


1 : FIRST TFT
2 : STORAGE CAPACITOR ELECTRODE
3 : CAPACITOR ELECTRODE
VL
DL
C1
BM1
12
GL
A
D
S
CL
8 : STORAGE CAPACITOR
C5
3 0 CONNECTION LINE
C4
C3
16
B
S
D
C2
2 0 : EL ELEMENT
GL
B
VL
6 : ANODE
4 : SECOND TFT
VL
1 5 : SECOND GATE ELECTRODE

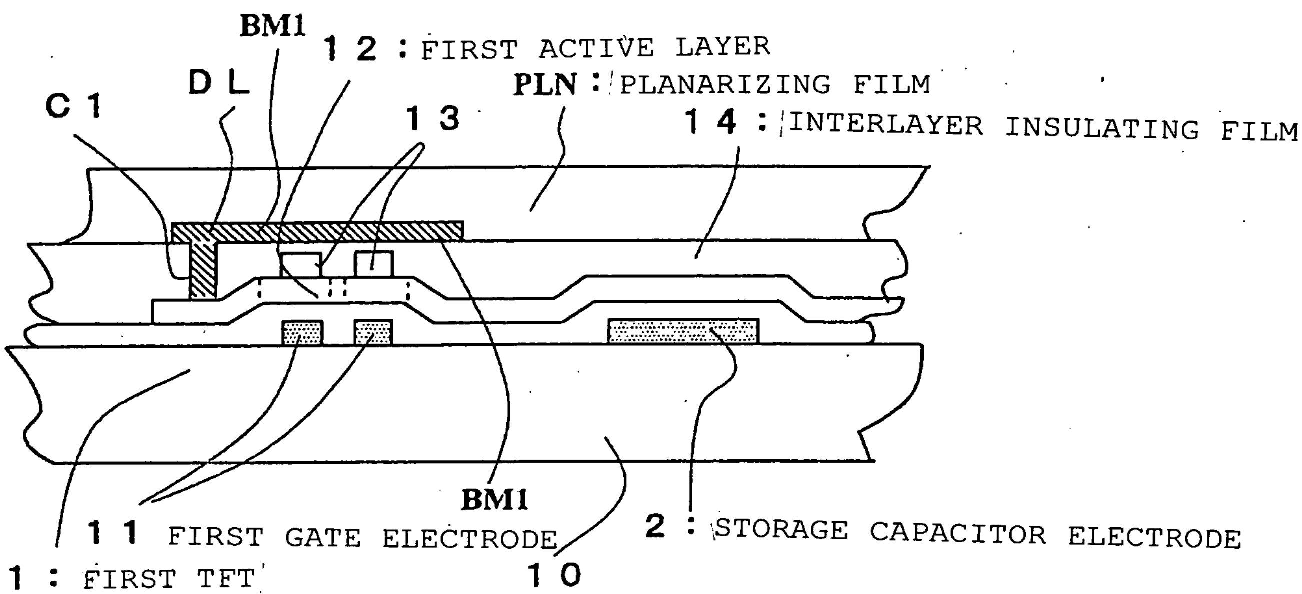
[Fig. 2]


３ : CAPACITOR ELECTRODE
１５ : SECOND GATE ELECTRODE
ＶＬ
３０ : CONNECTION LINE
C5
C4
F1
F2
F3
F4
C3
C2
S
D
6 : ANODE
IR1
IR2
4 : SECOND TFT
１６ : SECOND ACTIVE LAYER

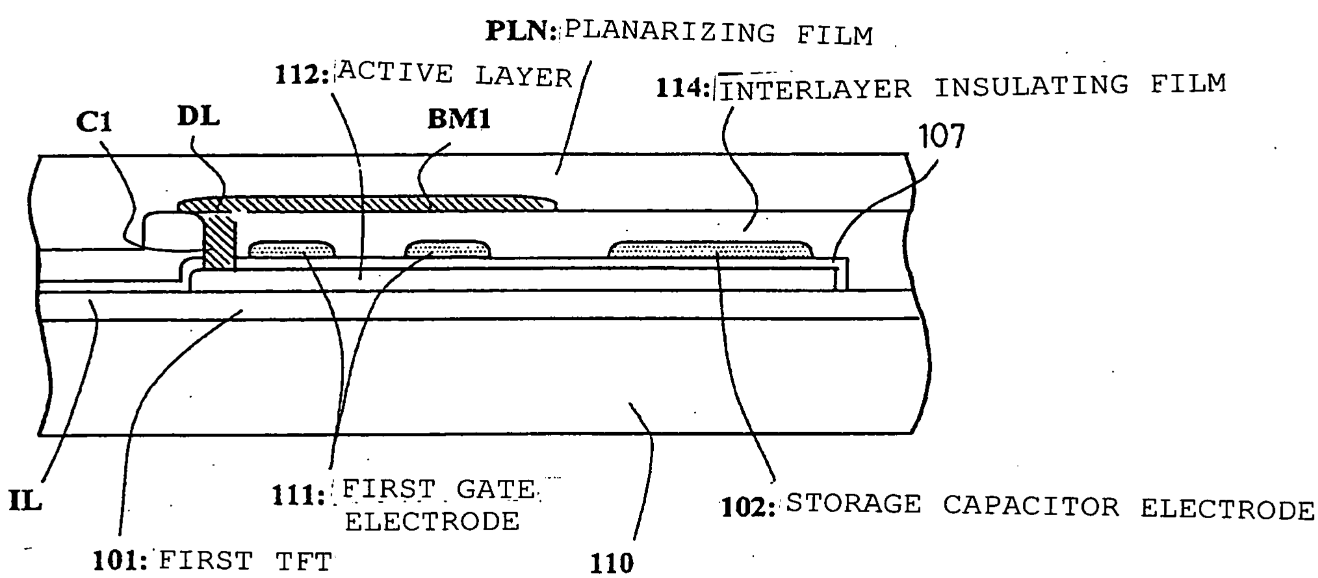
[Fig. 3]


CONNECTION
30 : LINE
VL
3 : CAPACITOR ELECTRODE
C4
C5
C3
C2
BM2
S
D
EM
24
23
22
21
6 : ANODE
25
BM2
4 : SECOND TFT
SE
C2
VL(DE)
i
C3
F1 F2 F3 F4
PLN
IR1
16
IR2
10
14 :
INTERLAYER INSULATING FILM
15 : SECOND GATE ELECTRODE

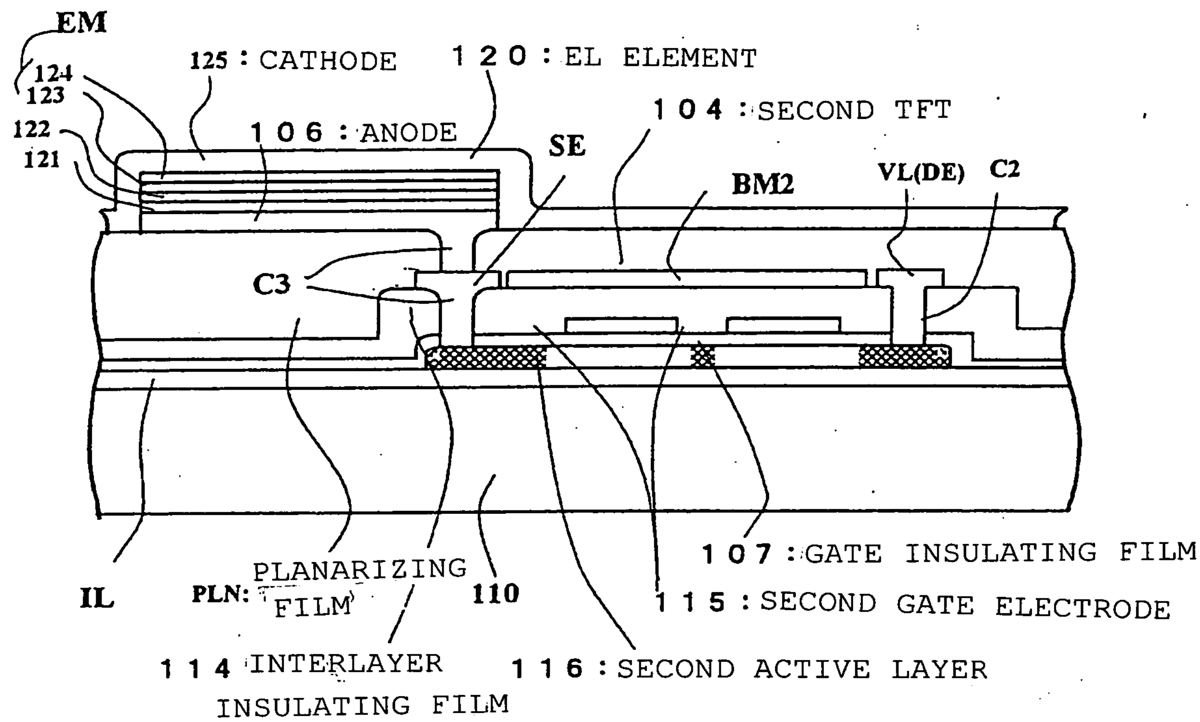
[Fig. 4]


BM1
1 2 : FIRST ACTIVE LAYER
D L
PLN : PLANARIZING FILM
C 1
1 3
1 4 : INTERLAYER INSULATING FILM
BM1
1 1 FIRST GATE ELECTRODE
2 : STORAGE CAPACITOR ELECTRODE
1 : FIRST TFT
1 0

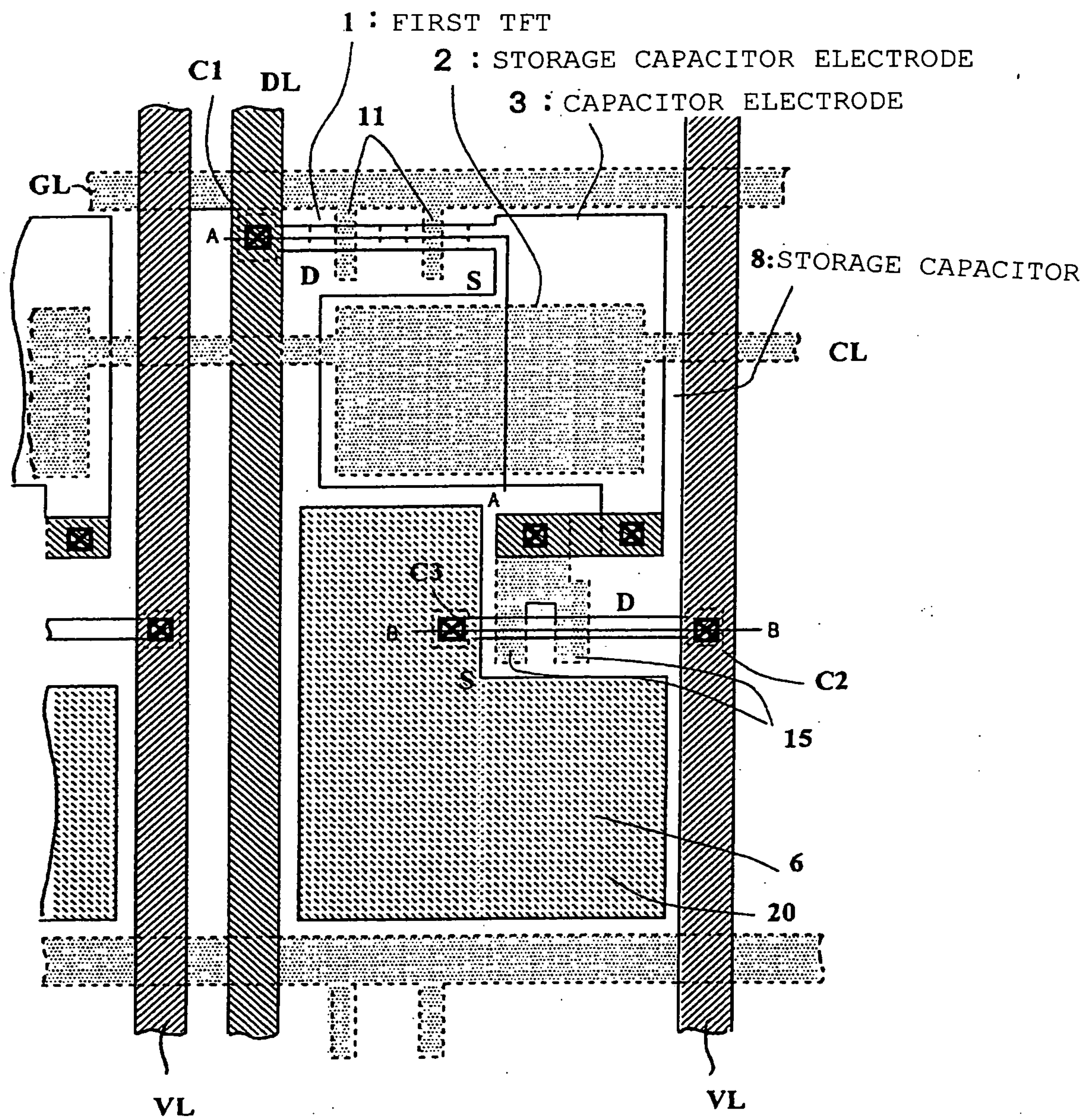
[Fig. 5]


PLN: PLANARIZING FILM
112: ACTIVE LAYER
114: INTERLAYER INSULATING FILM
C1
DL
BM1
107
IL
111: FIRST GATE ELECTRODE
102: STORAGE CAPACITOR ELECTRODE
101: FIRST TFT
110

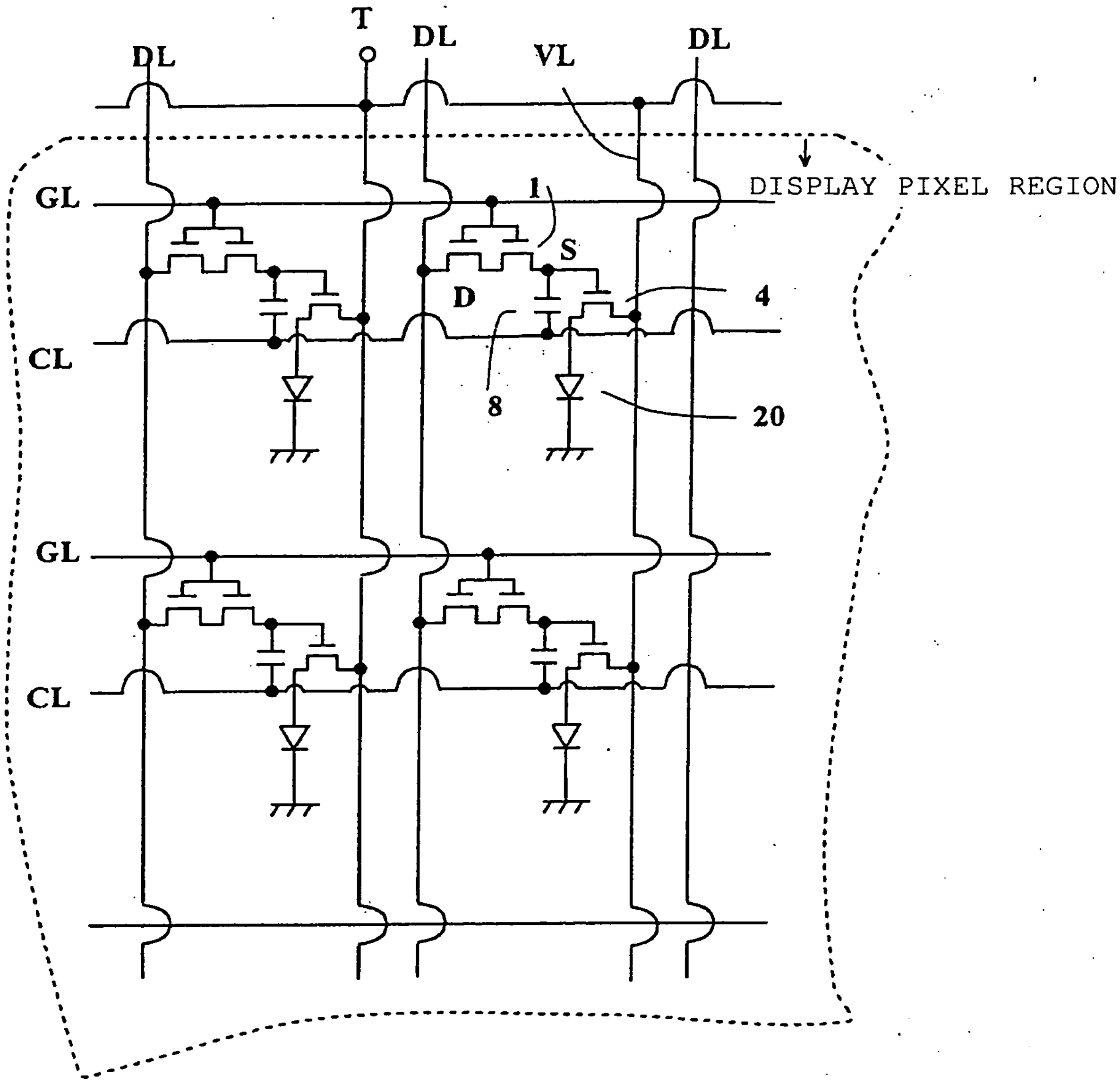
[Fig. 6]


EM
124
123
122
121
125 : CATHODE
1 2 0 : EL ELEMENT
1 0 6 : ANODE
1 0 4 : SECOND TFT
SE
BM2
VL(DE)
C2
C3
1 0 7 : GATE INSULATING FILM
IL
PLN: PLANARIZING FILM
110
1 1 5 : SECOND GATE ELECTRODE
1 1 4 INTERLAYER INSULATING FILM
1 1 6 : SECOND ACTIVE LAYER

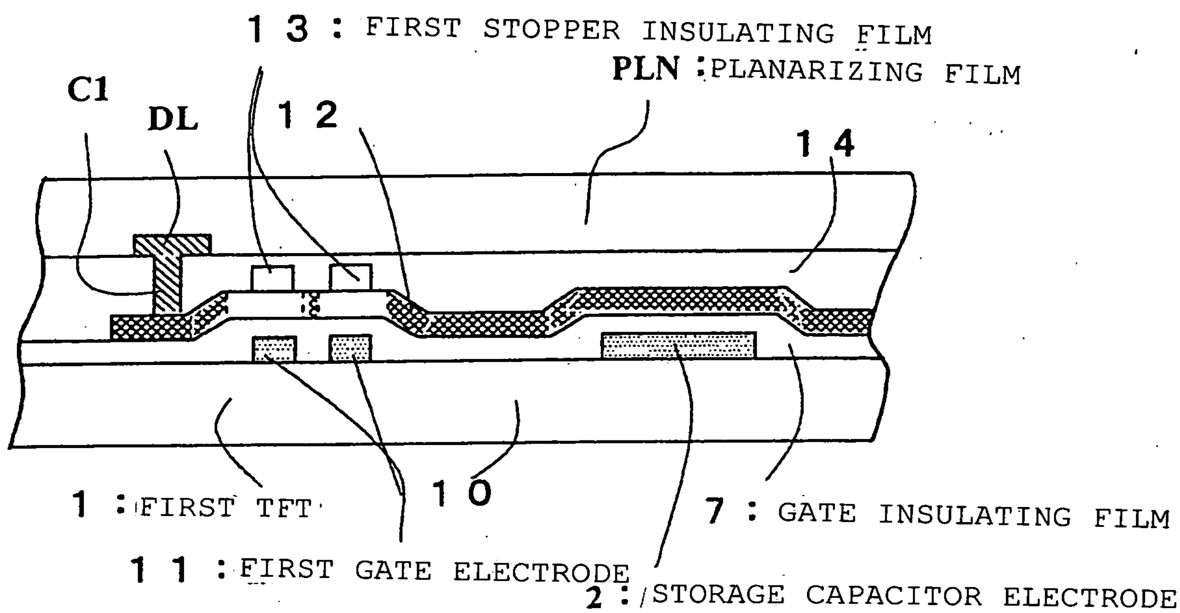
[Fig. 7]


1 : FIRST TFT
2 : STORAGE CAPACITOR ELECTRODE
3 : CAPACITOR ELECTRODE
8:STORAGE CAPACITOR
C1
DL
11
GL
A
D
S
CL
A
C3
D
B
B
C2
S
15
6
20
VL
VL

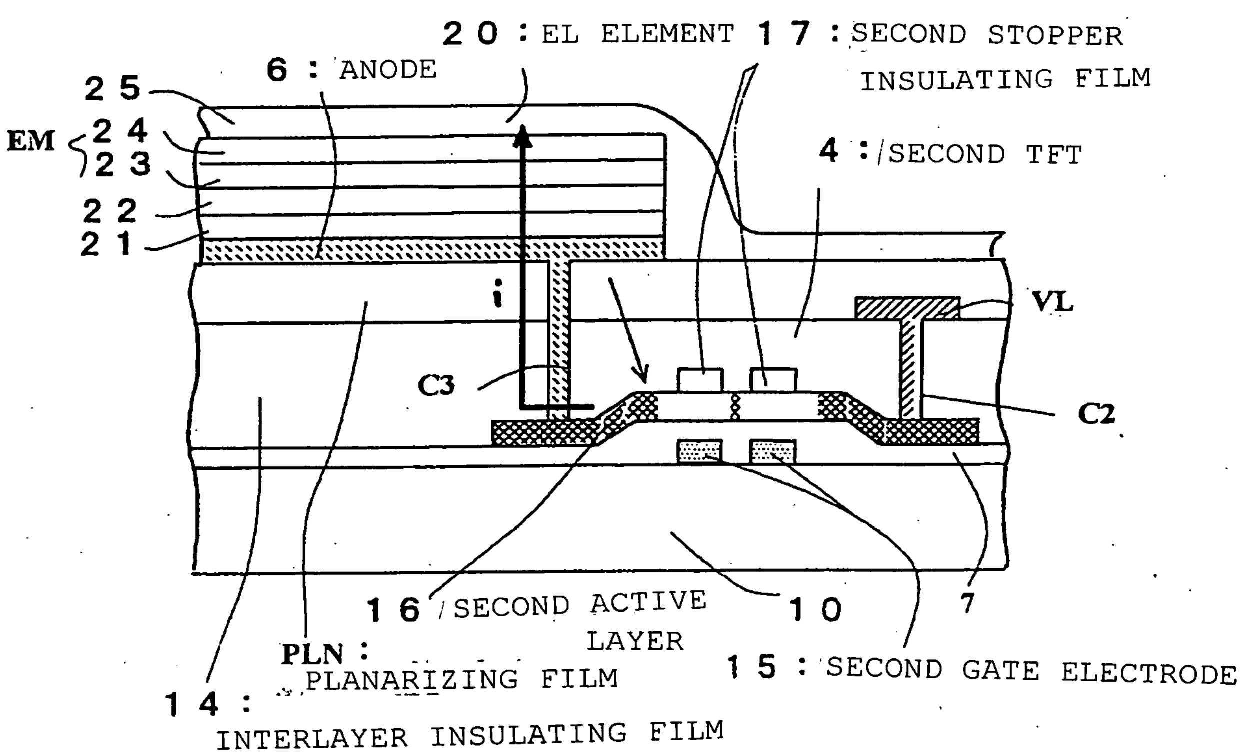
[Fig. 8]



[Fig. 9]


1 3 : FIRST STOPPER INSULATING FILM
PLN : PLANARIZING FILM
C1
DL
1 2
1 4
1 : FIRST TFT
1 0
7 : GATE INSULATING FILM
1 1 : FIRST GATE ELECTRODE
2 : /STORAGE CAPACITOR ELECTRODE

[Fig. 10]


2 0 : EL ELEMENT
1 7 : SECOND STOPPER INSULATING FILM
6 : ANODE
2 5
EM
2 4
2 3
2 2
2 1
4 : /SECOND TFT
VL
i
C3
C2
1 6 /SECOND ACTIVE LAYER
1 0
7
PLN : PLANARIZING FILM
1 5 : SECOND GATE ELECTRODE
1 4 : INTERLAYER INSULATING FILM

[Name of Document] Abstract

[Summary]

[Problem]

Because an EL element is self-emissive, there had been a problem in that the emitted light enters a TFT and generates a dark current which results in a brighter color than the original brightness of the EL element.

[Structure]

An EL element 20 and an interface F1 of diffusion region of a thin film transistor 4 close to the EL element are separated. A light shielding film BM2 is provided between the EL element 20 and the interface F1.

[Selected Drawing] Fig. 1